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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,667	10/01/2003	Soo-Guy Rho	9649-479CTDVCT2	8980

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EXAMINER	
CHOWDHURY, TARIFUR RASHID	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,667	RHO ET AL.	
	Examiner	Art Unit	
	Tarifur R Chowdhury	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/979,572.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 08/979,572, filed on 11/26/1997. ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 46 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the black matrix and the passivation layer and the pixel electrode.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 46-49, 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al., (Kim), USPAT 6,100,9540 in view of Zhang et al., (Zhang), USPAT 6,222,595.

6. Kim discloses (fifth preferred embodiment; col. 18, line 40- col. 19, line 40) and shows in Fig. 14C, a thin film transistor substrate for a liquid crystal display comprising:

- a first insulating substrate (111);
- a gate pattern including a gate and a gate line electrode (113) on the transparent insulating substrate (111);
- a gate insulating layer (157) on the gate electrode (113) and comprising organic insulating material;
- a patterned silicon nitride layer (177);
- a semiconductor layer (119) disposed on the gate insulating layer (157);
- a data pattern that comprises a source electrode (123) and a drain electrode (127), which are disposed on the semiconductor layer and a data line (125) that is connected to the drain electrode;
- a protection film (159) (applicant's passivation layer) that comprises organic insulating material (col. 18, line 67) and has a contact hole that exposes the drain electrode (127); and

- a pixel electrode (131) connected to the drain electrode (127) through the first contact hole.

Even though Kim does not explicitly show the second insulating substrate, inherently a liquid crystal display includes a second substrate facing the first substrate to sandwich the liquid crystal materials in between.

Kim differs from the claimed invention because he does not explicitly disclose the limitation such as a spacer is disposed at a region where a black matrix overlaps the gate line or the data line.

Zhang shows a conventional liquid crystal display wherein a spacer (112) is disposed at a region wherein a black matrix (108) overlaps the gate line (104) and the data line (106) (Fig. 1A).

Zhang is evidence that ordinary workers in the art would find a reason, suggestion or motivation to dispose a spacer at a region wherein a black matrix overlaps the gate line or the data line.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the display device of Kim by first forming a black matrix such that it overlaps either the gate line or the data line to prevent any light leakage between the signal lines and the pixel electrode and then form spacers at the region wherein the black matrix overlaps the gate line or the data line to determine the cell gap of the liquid crystal display.

Accordingly, claim 46 would have been obvious.

As to claim 47, Kim also discloses that the organic material used to form the passivation layer has superior properties of dielectric constant of 2.3 to 2.4 (col. 14, lines 10-12).

As to claim 48, Kim shows in Fig. 14C that the passivation layer (159) has a flat surface.

As to claim 49, Kim also shows in Fig. 14C that the pixel electrode (131) at least overlaps the data pattern.

As to claim 51, Kim discloses (col. 19, line 4-11) and shows in Fig. 14D that a etch stopper (135) is formed between the semiconductor layer (119) and the passivation layer (159).

As to claim 52, forming black matrix using photolithography is common and known in the art and thus would have been obvious to avail a proven technique.

7. Claims 46-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA).

8. The AAPA described in pages 1-3 and shown in Fig.1 of the present application discloses a thin film transistor substrate for a liquid crystal display comprising:

- a transparent insulating substrate (1);
- a gate pattern including a gate electrode (2) and a gate line (not shown) on the transparent insulating substrate (1);
- a gate insulating layer (4) on the gate electrode (2);
- a semiconductor layer (5) on the gate insulating layer (4);

- a source electrode (8) and a drain electrode (9), which are separated from each other on the semiconductor layer (5);
- a data line electrically connected to the source electrode (not shown);
- a passivation layer (10) having a first contact hole exposing the drain electrode (9); and
- a pixel electrode (12) connected to the drain electrode (9) through the first contact hole;

The AAPA described in the instant application also discloses that a second insulating substrate is placed opposite to the first insulating substrate and spacers are placed between the first insulating substrate and the second insulating substrate (page 2, line 22 – page 3, line 1).

The AAPA described in the instant application further discloses (page 2, line 17, page 3, line 10) and shows in Fig. 1 that a black matrix that overlaps the gate line or the data line is disposed in a groove of the passivation layer and spacers are disposed between the substrates to maintain a uniform cell gap. Further, since spacers are provided to keep an uniform gap between the substrates, it would have at least been obvious to one of ordinary skill in the art that the spacers are provided on top of the black matrix since the black matrix (11) is one of the top most layer of the insulating substrate (1).

The AAPA described in the instant application differs from the claimed invention because it does not explicitly disclose the limitation such as the passivation layer with flat surface comprising organic insulating material with low dielectric constant (such as

2.4-3.7). However, it is common and known in the art to use an organic material with low dielectric constant for forming a passivation layer with flat surface so that the pixel electrode can overlap the data pattern and thus an improved aperture ratio can be obtained. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ a passivation layer that has a flat surface and is made of an organic material having low dielectric constant so that the pixel electrode can overlap the data pattern and thus improved aperture ratio is obtained.

Accordingly, claims 46-50 would have been obvious.

As to claim 51, the AAPA described in the present application also shows in Figure 1 that an etch stopper (6) is formed between the passivation layer (10) and the semiconductor layer.

As to claim 52, forming black matrix using photolithography is common and known in the art and thus would have been obvious to avail a proven technique.

9. Claims 53-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al., (Shimada), USPAT 6,052,162.

10. Shimada discloses and shows in Figs. 1 and 5, a thin film transistor substrate for a liquid crystal display comprising:

- a transparent insulating substrate (31);
- a gate electrode (32) disposed on the first insulating substrate;
- a storage capacitor electrode (6) disposed on the insulating substrate;
- a gate insulating layer (33) that covers the gate line and the storage capacitor electrode (6);

- a semiconductor layer (34) disposed on the gate insulating layer (33);
- a data line (23) that crosses the gate line (22) and is disposed on the gate insulating layer (33);
- a metal pattern (41) that is disposed over the storage capacitor electrode (6);
- a passivation layer (38) that comprises organic insulating material having a dielectric constant of 3.4 to 3.8 (col. 9, lines 4-5) (overlaps the claimed range) and is disposed on the semiconductor layer (34) and the data line (23), and has a contact hole (26b) that exposes the metal pattern (41); and
- a pixel electrode (21) connected to the metal pattern 941) through the contact hole (26b).

Shimada differs from the claimed invention because he does not explicitly disclose that the metal pattern is disposed on the same layer with the data line. However, it is a standard practice in the liquid crystal art to reduce manufacturing steps for cost effectiveness. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to dispose the metal pattern on the same layer with the data line so that an extra step to form the metal pattern is eliminated and thus manufacturing step is reduced and thus the cost.

Accordingly, claims 53 and 54 would have been obvious.

As to claim 55, Shimada shows in Fig. 5 that the passivation layer (38) has a flat surface.

As to claim 56, even though Shimada does not explicitly disclose that the pixel electrode overlaps at least a portion of the data line, it is common and known in the art

that when pixel electrode overlaps the data line aperture ratio is increased and thus it would have been obvious.

As to claim 57, Shimada also shows in Fig. 5 that the thin film transistor substrate further comprising a channel protection layer (35) (applicant's etch stopping layer) that is disposed between the semiconductor layer (34) and the passivation layer (38).

Double Patenting

11. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

12. Claims 53-57 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 41-49 of U.S. Patent No. 6,597,415. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patented claims anticipate the instant claims.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) USPAT 5,933,208 is related to a liquid crystal display device wherein the light shielding layer and the color filter form a substantially planarized surface over the TFT.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tarifur R Chowdhury whose telephone number is (571) 272-2287. The examiner can normally be reached on M-Th (6:30-5:00) Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRC
April 14, 2003

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER